ATLAS/Lar calibration system

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ATLAS / LAr calibration system

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Abstract

The liquid Argon calibration board has been designed to deliver a uniform, stable and linear signal whose shape is similar to the calorimeter ionisation current signal over 16 bits dynamic range. 3 versions of boards with 128 pulse generators have been built using DMILL components.

The performances have been measured on the last prototype (amplitude and timing measurements, linearity, uniformity, jitters, …) and will be presented in detail.

Boards qualification for the whole production next year will be described.

I. Introduction

The liquid argon calorimeter is designed to reconstruct the energy and the position of electrons, photons and jets [1]. To reach this goal, physics requires an excellent energy resolution, a large dynamic range and a very fast response. Moreover, it will be necessary to obtain a good radiation tolerance. These constraints define the characteristics of the calibration board.

The energy resolution obtained with a prototype in beam test is given below:

$$\frac{\sigma_E}{E} = \frac{10\%}{\sqrt{E}} \oplus \frac{300\text{MeV}}{E} \oplus 0.7\%$$

The constant term of 0.7%, which includes the non-uniformity of the energy response, is the goal determined for the final calorimeter. Among the non-uniformity sources which can contribute to this constant term, the main contribution comes from the electronics readout (0.25%). It is directly linked to our ability to calibrate the 200000 channels of the calorimeter with a good accuracy.

The LAr calibration boards, which are located right on the cryostat in dedicated front-end crates, house 128 pulsers which generate accurate pulses to simulate the detector signal over the full 16 bits dynamic range.

This paper reminds the requirements and the principle of the calibration, describes the performances of the last prototype and presents the qualification procedure for the whole production.

II. Requirements and principle

A. Requirements

The calibration board [2] is designed to inject a current pulse as close as possible as the physics pulse over the full dynamic range (from 2µA to 200 mA). It includes 128 analog channels delivering fast pulses (rise time below 1 ns) with a 450 ns exponential decay. The accuracy of the calibration must be good and so the integral non linearity lower than 0.1% and the non uniformity between channels better than 0.25%. The timing between real physics signal and the calibration pulse must be within ±1 ns. The jitter introduced by the board must be better than the one induced by the arrival time of the particles, around 150 ps. The radiation levels anticipated at the LAr crate location is 50 Gy in 10 years and 1.6 10^{12} N/cm^2. The first prototype using COTS components has been realised to validate the architecture, but the final development is based on a completely radiation tolerant version, by migrating the active elements into DMILL ASICs. Taking into account the safety factors required by the radiation tolerance policy [3], these chips must be qualified up to 500 Gy and 1.6 10^{13} N/cm^2.

B. Principle

1) Analog part

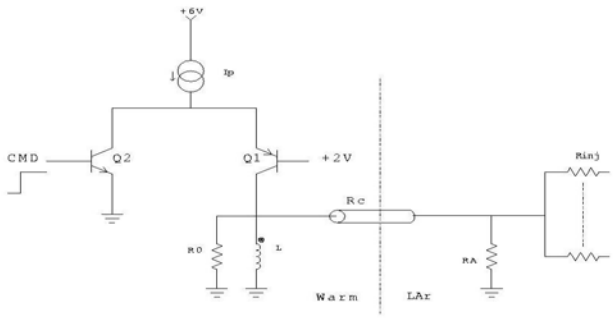

Figure 1: Pulser principle

The fast output voltage pulse is obtained by interrupting a precise DC current that flows in the inductor (figure 1.).

When a fast TTL command pulse is applied on the NPN transistor, the PMOS transistor is off and the current is diverted to ground. The magnetic energy stored in the inductor produces a voltage pulse with an exponential decay.

To generate the precise DC current from 2µA to 200 mA, a 16 bit DAC is necessary. The DAC voltage which varies from 16 µV to 1 V is distributed to the 128 pulsers thanks to a low offset operational amplifier in voltage follower configuration. The voltage to current conversion is built upon a low offset operational amplifier in voltage to current converter configuration and a precise 0.1% 5 Ω resistor.

2) Digital part

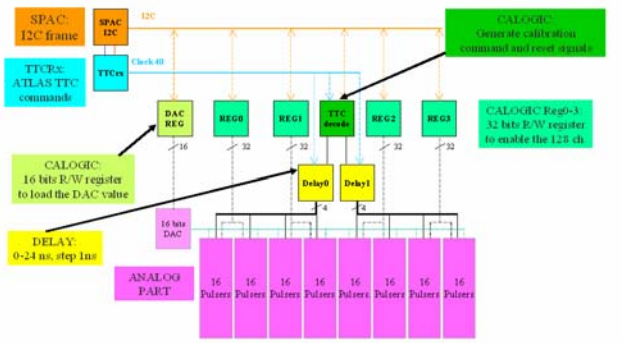

Figure 2: Schematics of the digital part

A dedicated DMILL chip (CALOGIC [4]) is designed to manage the board control logic (figure 2.). The digital part receives the 40 MHz clock from the TTC system (Timing Trigger Control) and decode the calibration command.

On the other hand, this chip manages external communications via a dedicated serial protocol (I2C). This allows to enable desired channels via 32 bits output registers (REG0-3). It is also possible to load a DAC value via a 16 bits output register. In order to compensate the cable lengths, the calibration command can be delayed by step of 1 ns between 0 and 24 ns. Moreover, the chip allows to control the voltage regulators and to monitor the temperature.

3) Board design

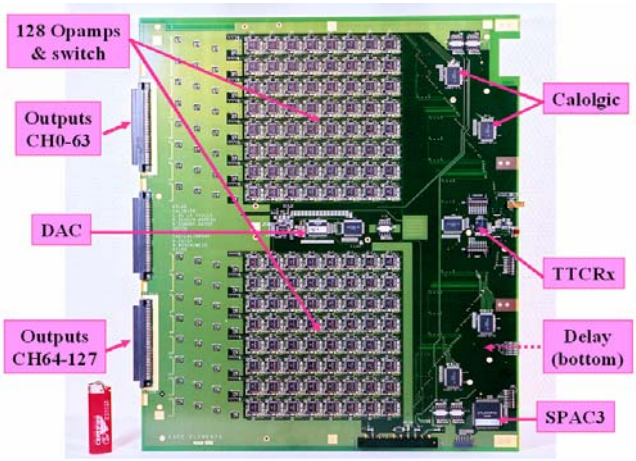

Figure 3: Calibration board

The size of the board (49.5 x 40.5 cm) and the number of channels (128) have been determined by the front-end crate design. The calibration board is divided in two groups of 8 rows of 8 operational amplifiers (figure 3.). The challenge is to obtain a uniform distribution in time and in amplitude with a very high density of components. Another difficulty is to minimize the coupling between channels or between the digital and sensitive analog signals.

III. PERFORMANCES OF LAST PROTOTYPE

A. Amplitude measurements

1) DC measurements

One DAC per board is distributed to the 128 channels. The DAC linearity has been measured on the 3 shaper scales (high gain = 0-10 mV, medium gain = 0-100 mV, low gain = 0-1 V) with a precise voltmeter. The residuals plots are presented in figure 4.

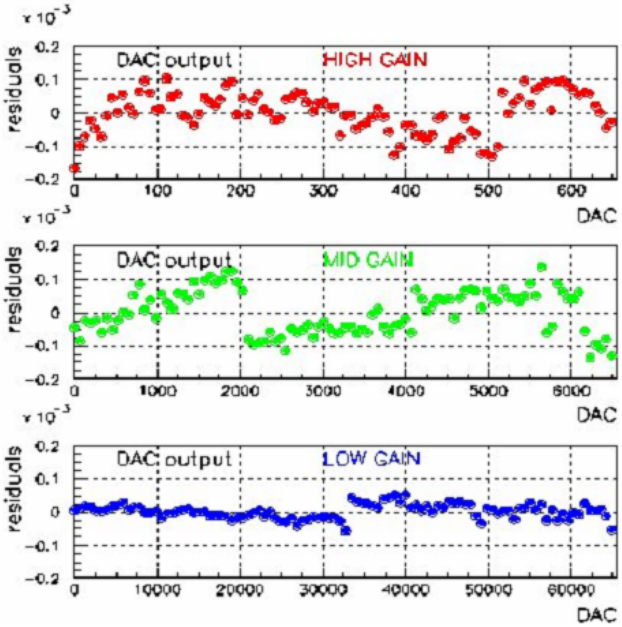

Figure 4: Residuals of DAC linearity over the 3 shaper scales

We obtain an excellent non-linearity which do not exceed 0.01% in each gain, far better than the requirement of 0.1%. In the different gains, we easily observe the bit structure. The parameters of DAC linearity result from a linear fit over 100 DAC values: the offset, varying from 16 µV to 25 µV, comes mainly from the distribution operational amplifier and the gain corresponds to 1 LSB=15,26µV.

The DC output current linearity has been performed only on one channel on the 3 scales. The residuals are also lower than 0.01% and show a similar pattern as the DAC residuals. So the linearity is not affected by the signal distribution to the 128 output channels. Moreover, we have compared the parameters of DC current linearity when 1 or 128 channels are ON. The results are roughly similar in both cases.

The DC current uniformity on 128 channels has been measured at the full scale of the high gain and medium gain, and is presented in figure 5.

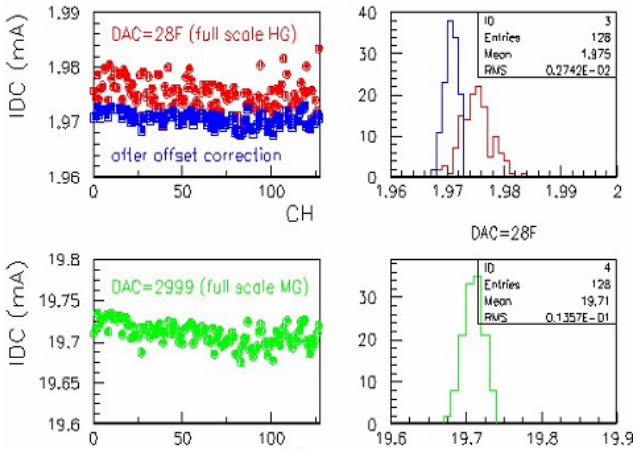

Figure 5: DC uniformity for high and middle gains at full scale

The non-uniformity in high gain is dominated by the operational amplifier offsets with a dispersion of 0.14% which becomes 0.06% after correction. In the medium gain, the offsets are no longer visible and the dispersion amounts to a similar value (0.07%), dominated by the accuracy on the discrete components.

2) Dynamic measurements

The dynamic measurements use a dedicated hardware based on a multiplexor to scan automatically the 128 channels, a shaper CR-RC2 (time constant = 50 ns) and a readout system with a 12 bits ADC. The amplitude is measured at the signal peak averaged on 100 triggers. The multiplexor has been qualified independently and shows a dispersion of 0.05% on the 128 channels.

The linearity after shaping has been measured over the 3 gains, and the residuals are presented in figure 6.

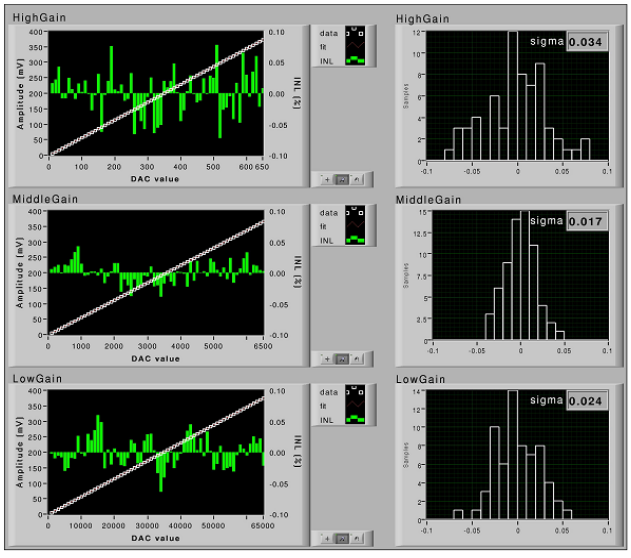

Figure 6: Integral non-linearity of the amplitude over the 3 gains

The integral non-linearity is within ±0.1% for all gains. We notice that the dynamic linearity is worse by a factor about ten compared to the DC current measurements: a contribution to this effect comes from the non-linearity of the readout used. Nevertheless, the results are better than the 0.1% required.

The uniformity of the amplitude over the 128 channels has been measured at DAC=10000 and is presented in figure 7.

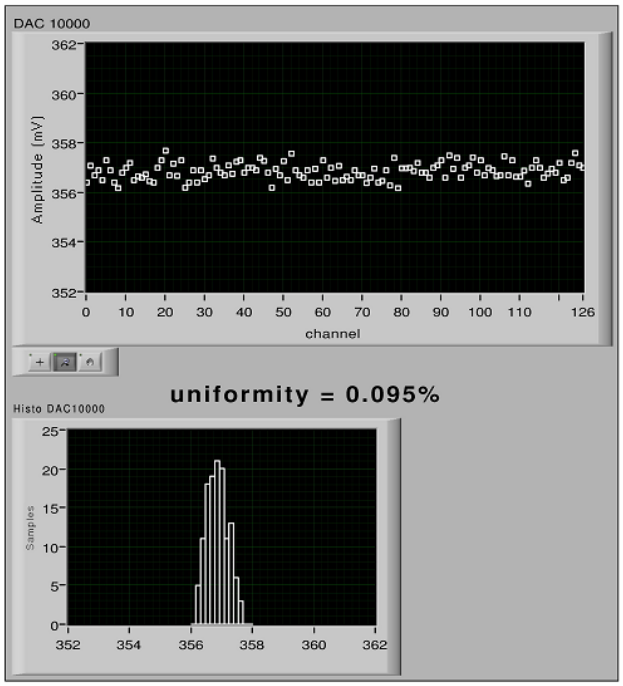

Figure 7: Amplitude uniformity for DAC=10000

A dispersion of 0.095% is obtained, larger than the value of 0.07% obtained with the DC measurements. It can be attributed to the inductances dispersion and to the small dispersion of the output lines. The same uniformity is obtained whatever the DAC setting due to its excellent linearity. But once again, this result is far better than the requirements of 0.25%.

B. Timing measurements

The delay between the LV1A (trigger) and the calibration pulse is settled by two ways. With the PHOS4-RH delay chip, it is possible to delay 4 bulks of 16 calibration channels between 0 and 24 ns by step of 1 ns. This chip is used to compensate for cable lengths across the calorimeter. With the TTCrx fine delay, we have one unique delay value between 0 and 24 ns by step of 104 ps for the 128 channels. It is used to scan the calibration pulse during special runs. The purpose of the timing measurements is to characterize the timing of the full calibration chain. The characteristics have been investigated with an accuracy oscilloscope (16 GS/s, 1 GHz) which gives the possibility to record histograms of the delay between the 40 MHz clock and the outputs of the board channels. The intercept, the slope and the averaged jitter are extracted from linear fit.

1) Timing linearity

The timing linearity scanning the PHOS4-RH delay values has been preceded by a specific chip study [5]. Indeed, a dependence of the chip performances with temperature or supply voltage has been identified. The whole production (approximately 600 chips) has been tested in a monitored environment. After that, the chips have been selected on jitter and sorted on the step value. The fit representing the measured average value and the jitter versus the expected delay value are shown in figure 8.

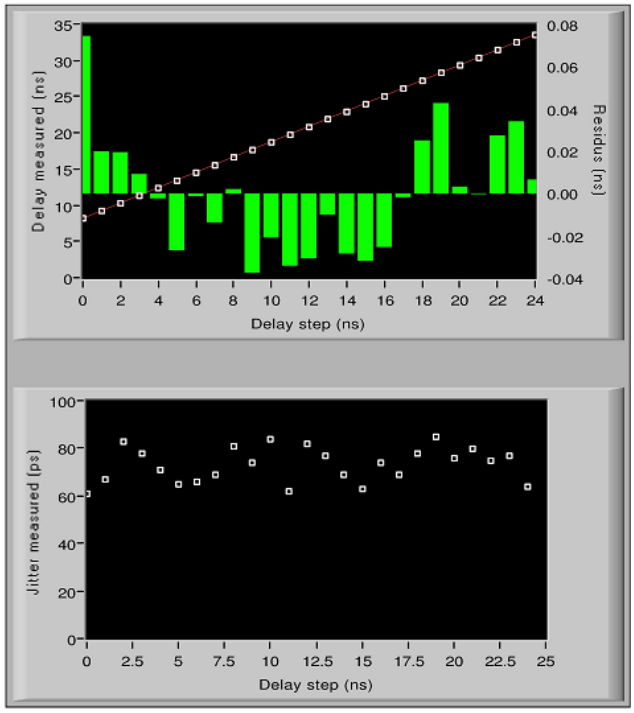

Figure 8: Linearity measurement with PHOS4-RH delay chip

The slope and the shape of the non-linearity depend on the PHOS4-RH channel, the chip and the temperature. Consequently, the slope is not exactly equal to 1, as we had seen in the preliminary study. On the other hand, the maximum non-linearity is smaller than 70 ps. So it is possible to obtain a precise and stable delay value after a chip calibration. Concerning the jitter, we measure an average of 75 ps, in good agreement with the requirements (< 150 ps). This jitter is stable whatever the delay value due to the chip selection. Of course, these performances are true if we keep the operation point below a temperature threshold with a good cooling.

The timing linearity with the TTCrx fine delay is shown in figure 9. With this chip, the slope of the fit is equal to 1 to better than 1%. The non-linearity of ±250 ps is similar to the TTCrx datasheet. The jitter is stable whatever the fine delay value and in average equal to 75 ps.

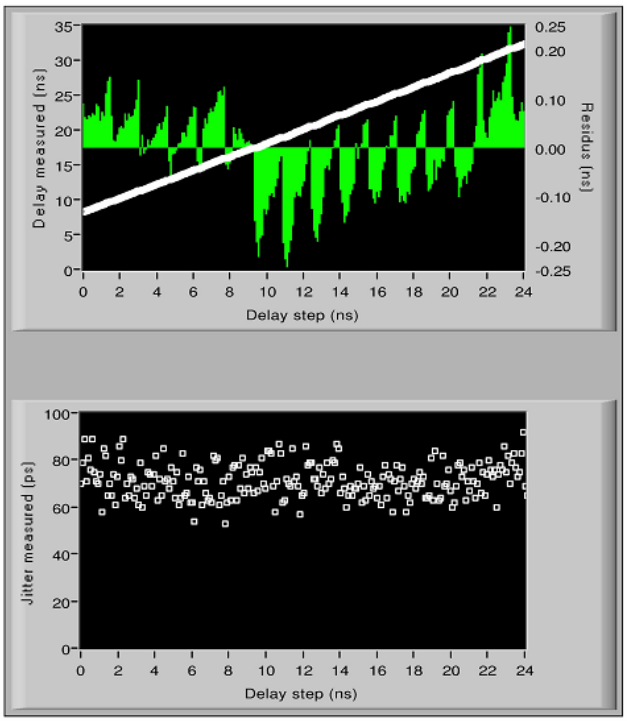

Figure 9: Linearity measurement with TTCrx delay chip

2) Timing uniformity

The purpose of this test is to measure the timing response of all the calibration board channels scanning the delay values of the PHOS4-RH from 0 to 24 ns. The intercept, the slope and the mean jitter of the linear fit are recorded for each calibration channel.

The plot of the intercept is shown in figure 10.

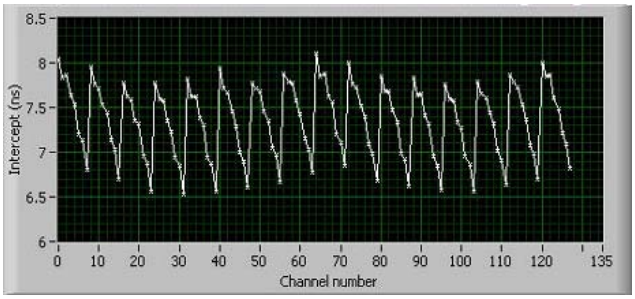

Figure 10: Time intercept uniformity versus channel number

We observe a dispersion inside a same row of 8 operational amplifiers, due to the fact that one calibration line distributes one row of 8 operational amplifiers. A parabolic behavior by group of 64 channels is visible, corresponding to the different output lengths at the connector level. Finally, an offset by group of 16 channels is induced by each PHOS4-RH output, but this little effect is submerged by the parabolic behavior.

The jitter is stable whatever the calibration channel. It is found around 75 ps, in agreement with the requirements.

The plot of the slope is presented in figure 11.

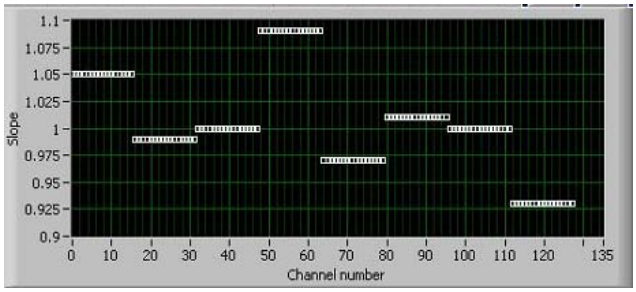

Figure 11: Delay chip slope uniformity versus channel number

The slope value is stable by group of 16 channels because one line drives 16 calibration channels. The dispersion by group of 16 channels is an intrinsic characteristics of the PHOS4-RH delay chips. The slope variation reaches 15% and that is why we will need to correct the values from numbers stored in a database. But these chips will be used only for global timing adjusting. An excellent accuracy is not necessary.

IV. PRODUCTION, TESTS AND QUALIFICATION

A. Board qualification procedure

The first step to qualify the production is made in industry. A visual inspection after assembling, a measurement of the power supply consumption and a burn-in test is expected.

The second step is performed in laboratory. First, the traceability is insured by the identification of the whole chips on the board. Indeed, all the chips characteristics are saved in a database in order to correlate them with the measurements on the calibration boards themselves. Then, the board is powered up and the current is measured and compared to the measurement done before burn-in at the assembly firm. The digital part is tested and several parameters are tuned (voltage regulators, DAC scale).

Finally, the precision measurements are performed. The operational amplifiers offsets, the inductor resistances, the decay time constant of the exponential calibration are measured. The linearity of all channels and the uniformity over the 3 gains is determined. The delay chips are characterized (offset, slope, jitter) and the TTCrx fine delay is monitored.

B. Test bench setup

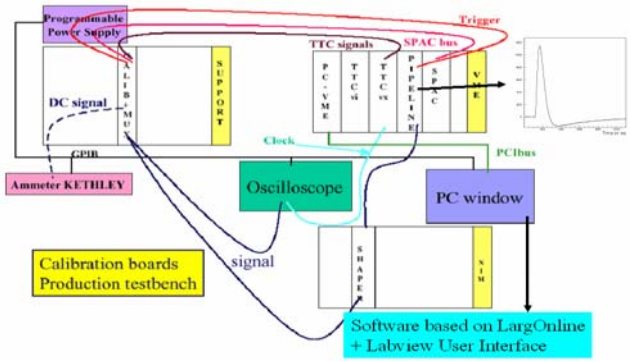

Figure 12: Test bench setup

A calibrated test bench is mandatory to qualify the whole production in the same conditions with an accuracy as good as 0.1%. Indeed a change in the scale of the signal of one board will introduce an energy scale variation in the region of the calorimeter pulsed by this board. Moreover, an automatic procedure is necessary taking into account the numerous parameters to be measured (figure 12.).

The test bench consists in:

- A PC with a PCI interface to manage a VME bus and a GPIB bus.
- A VME crate which holds the VME controller, a SPAC master, the TTCvi and TTCvx modules, and the digitizing board for the amplitude dynamic measurements.
- A shaper module (CR-RC2) to obtain a pulse with a peaking time around 40 ns.
- A programmable power supply with currents readout.
- A multiplexor to scan the 128 channels of the calibration board.
- A precise multimeter for the DC measurements.
- An accuracy oscilloscope for timing measurements.
- A LabVIEW program for the devices control, the user interface, the analysis and the data storage.

V. CONCLUSION

Extensive tests and measurements have been done in order to fulfill the calorimeter requirements. Ten non radhard boards produced in 1998 have been successfully tested during five years in beam tests. The DMILL chips (DAC, pulser, control logic, delay) designed in 1999-2001 exhibit good performances. Finally, three versions of radiation hard boards have been produced in 2002-2003 and the last prototype is in operation at the CERN combined run this summer.

All the components are now produced and tested. The selection is in progress. A pre-series of 4 calibration boards is waited for tests of final ATLAS calorimeter electronics next october.

Finally, the production of 130 boards for ATLAS is foreseen beginning 2005 and the installation in the pit on the calorimeter at CERN will be done in spring 2005.

VI. REFERENCES

[1] LAr Technical Design Report. CERN/LHCC/96-41

[2] The Liquid Argon Calorimeter Calibration Board. ATL-LARG-2000-006

[3] ATLAS Policy on Radiation Tolerant Electronics. ATC-TE-QA-0001

[4] The ATLAS LARG Calorimeter Digital Calibration ASIC. wwwlapp.in2p3.fr/atlas/Electronique/Calibration/System/

[5] ATLAS Calibration delay study. ATL-ELEC-2004-001